

CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

- 1 *Sub a* 1. An integrated circuit including an embedded
2 memory and a built-in self-test arrangement
3 including
4 means for storing test instructions including
5 means for receiving test instructions provided from
6 an external tester,
7 means for generating default test instructions,
8 and
9 means for supplying said default test
10 instructions to said means for storing test
11 instructions.
- 1 2. An integrated circuit as recited in claim 1,
2 wherein said *means* for generating default test
3 instructions includes an initialization storage
4 means.
- Sub C2* 1 3. An integrated circuit as recited in claim 2,
2 wherein said initialization storage means is a
3 storage initialization module.

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1 ~~8.~~ An electronic system including an integrated
2 circuit having a built-in self-test arrangement
3 therein, said integrated circuit including
4 means for storing test instructions including
5 means for receiving test instructions provided from
6 an external tester,
7 means for generating default test instructions,
8 and
9 means for supplying said default test
10 instructions to said means for storing test
11 instructions.

1 9. A system as recited in claim 8, wherein said
2 means for generating default test instructions
3 includes an initialization storage means.

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1 10. A system as recited in claim 9, wherein said
2 initialization storage means is a storage
3 initialization module.

1 11. A system as recited in claim 8, further
2 including
3 means for activating said means for generating
4 said default test instructions responsive to an
5 absence of test instructions from an external
6 tester.

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1 13. A system as recited in claim 12, further
2 including
3 means for activating said means for generating
4 said default test instructions when only said
5 control signal is supplied to said instruction
6 storage controller.

1 14. A system as recited in claim 12, wherein said
2 control signal is supplied from an external tester.

1 15. A system as recited in claim 12, wherein said
2 control signal is supplied from within said system.

1 16. A system as recited in claim 8, wherein said
2 means for generating default test instructions
3 includes a memory for storing said default test
4 instructions.

17. A method of performing system level tests on an electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level and board level testing and including means for storing a test algorithm, said method comprising steps of

- providing a system level test algorithm from said BIST arrangement,
- transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and
- operating said BIST arrangement using said system level test algorithm.